WF-2538

FINAL REPORT

ON

JPL STAIRCASE GENERATOR MODULE

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CONTRACT NO. 950012 NASW-6

Prepared for

JET PROPULSION LABORATORY

PASADENA 3, CALIFORNIA

SOLID STATE ELECTRONICS DEPARTMENT

MOTOROLA INC.
WESTERN CENTER
Military Electronics Division

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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

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ABSTRACT

27270

Motorola has fabricated three staircase generator circuits (each consisting of a R-C Clock, six binary counters, and a summing network) by integrated thin-film methods. Interconnections between submodules are provided by a flexible printed wiring board.

The object is to provide circuits having the smallest weight, least volume, and lowest power consumption compatible with high reliability, producibility, accessibility and cost.

A high degree of accessibility is provided. Thin-film submodules may be replaced without damage to themselves or the printed wiring board. Diodes and transistors may be changed on the thin-film R-C submodules.

Author

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SECTION 1

1. INTRODUCTION

This report covers the period from 22 August 1960 through 29 September 1961 for Contract No. 950012 NASW-6.

1.1 OBJECTIVE

The objective of this program has been to construct and deliver to JPL three thin-film, integrated circuit, staircase generators, to demonstrate the advantages offered by this manufacturing method to the field of space electronics. A staircase voltage generator circuit supplied by JPL was adapted to utilize thin-film integrated circuit techniques developed at Motorola. These techniques provide equipments having the smallest volume, and the least weight and power consumption compatible with circuit reliability, producibility, and cost.

1.2 INITIAL PHASE

The initial phase of the contract covered by this report included circuit design and breadboard evaluation of the JPL staircase generator, in addition to the proposed equivalent thin-film integrated circuit design layout.

The electrical characteristics of the staircase generator are similar to those of the circuit (Figure 1) as supplied by JPL:

(1) The output consists of a repetitive stairstep waveform having 64 equally spaced potential steps between and including the minimum and maximum voltages.
(2) The clock signal for these steps is produced by a free-running astable multivibrator whose frequency is between 1 and 100 cps.
(3) A total of six binary counters and associated clamp circuits are employed to sum voltages obtained from a zener diode voltage reference using a resistor network.

1.3 CIRCUIT DESIGN AND EVALUATION PHASE

Motorola evaluated the staircase generator circuit supplied by JPL and made minor modifications to improve the producibility of a thin-film microelectronic equivalent. The modified circuit diagram is shown in Figure 2. The total power drain has been reduced by nearly 50 per cent, by dropping the supply voltage from 15 to 6 volts. The lower reference voltage also allowed for a large reduction in the summing resistor network values, thereby reducing the volume and weight of these elements. This is feasible because Motorola Semiconductor Division has available a 2.0-volt zener reference element. The resulting output potential (0 to 94.5 mv across a 5000-ohm load) is suitable for driving a direct-coupled voltage amplifier. The internal 5000-ohm resistor may be disconnected when feeding an amplifier that includes a suitable load.

Another minor modification was the substitution of NPN silicon transistors for PNP units in the astable clock circuit. PNP uncased transistor elements were not readily available; however, uncased NPN units were available from at least four suppliers.

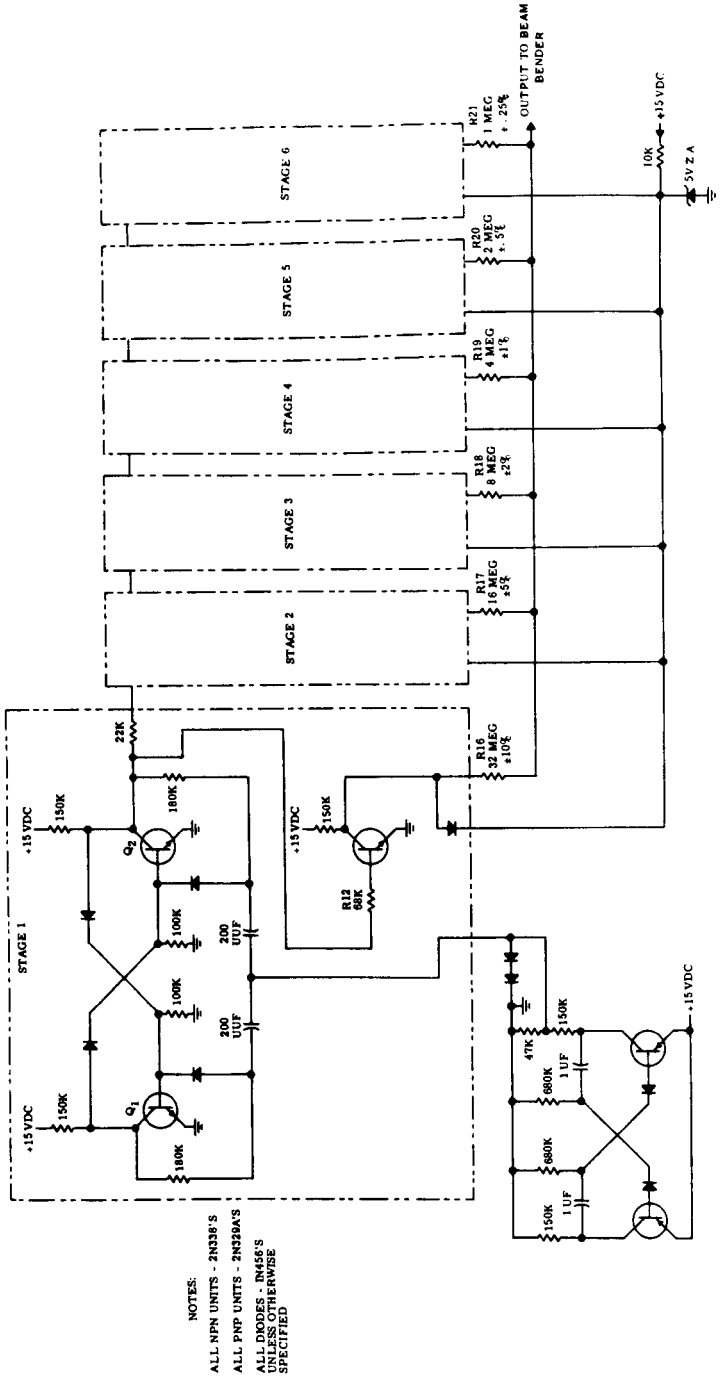

Figure 1. JPL Circuit Diagram

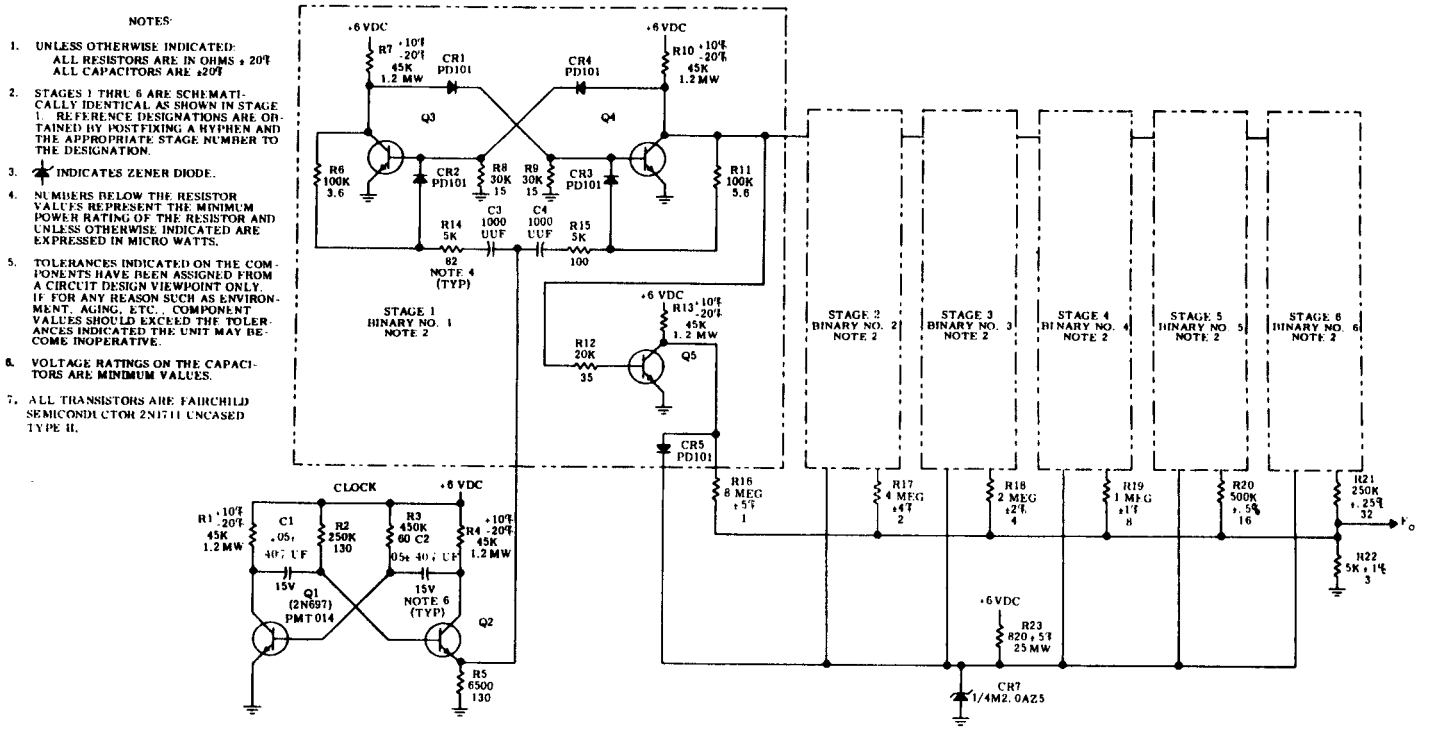

Figure 2. Modified Circuit Diagram

A breadboard of the modified circuit (Figure 2) constructed with conventional components was evaluated to determine component center values and tolerances. The breadboard circuit operated satisfactorily over a temperature range of -20 C to +55 C.

The following circuit specifications have been determined for the power source and for the stairstep output:

(1) Power input: 6.0 volts ±20 per cent at 7.2 ma. (Of the 7.2 ma, 5.0 ma is required to establish a reference voltage.)

(2) Stairstep output: The output amplitude of the 63rd step shall be 94.5 mv ±5 per cent measured across a 5000-ohm load.

Each step shall be within ±5 per cent of the nominal value of 1.5 mv per step.

1.4 JPL CONTRACT CONFERENCE

A conference was held at Motorola on 18 November 1960, to discuss this program. JPL was represented by Mr. Heacock, Mr. Allen, Mr. Hyser, and Mr. Nichols.

The breadboard circuit was demonstrated and a tour of the Integrated Circuits Laboratory was provided to show Motorola's thin-film circuit fabrication methods.

Packaging methods were presented in considerable detail. JPL felt that the solid encapsulated block of stacked submodules was not an acceptable packaging method since the circuits must be accessible down to submodules as well as diodes and transistors. Motorola's folded flexible printed wiring board modular assembly plan satisfied all requirements.

SECTION 2

2. THIN-FILM CIRCUIT DESIGN

The staircase generator circuit was divided into functional submodules, as shown in Figure 2. Thin-film layouts were made, active elements chosen, and test procedures prepared, as discussed in the following sections.

2.1 BASIC CIRCUIT MODULES

The voltage staircase generator consists of nine submodules with the following circuit functions:

(1) Basic clock astable multivibrator circuit placed on one substrate.

(2) Clock timing capacitors on one substrate to set the clock frequency.

(3) Six binary counters and associated clamp circuits, each on one substrate.

(4) A 4-and an 8-megohm resistor together on one substrate.

The remaining summing resistors and zener reference diode are purchased, rather than fabricated by thin-film techniques.

2.2 THIN-FILM COMPONENTS

Resistors are formed by first coating the substrate with a thin film of tin oxide, followed by a photo-resist etching process to delineate the desired resistor pattern. A film resistance of 5000 ohms per square is utilized for all resistors.

A conductor pattern is created on a substrate by the vacuum evaporation of chrome-gold alloy through a metallic mask.

Tantalum film is deposited through a metallic mask to provide substrate electrodes and then anodized for the capacitor dielectric in the construction of the bistable circuit.

Counterelectrodes for the capacitors are provided by a chrome-gold film evaporated through a metallic mask. Tantalum film capacitors are utilized in the clock timing circuit because they provide a large capacitance value per unit substrate area. These are constructed by the anodization of a tantalum film and the deposition of a chrome-gold alloy counterelectrode.

2.3 ACTIVE ELEMENTS

The submodules are designed for Pacific Semiconductor PD101 micro-diodes and Fairchild Semiconductor 2N1711 uncased transistors. These transistors are similar in characteristics to the 2N697 type. A saturation voltage of less than 0.2 volt is considered acceptable for these transistors. A simple test circuit providing 100 microamperes for the collector and 10 microamperes for the base is used to check the saturation characteristic.

2.4 THIN-FILM CIRCUIT DESIGN

The design parameters presented in Section 2.2 have been utilized to convert the breadboard circuit to thin-film integrated circuit layouts.

Each submodule is constructed on a fotoceram substrate 0.5 x 0.5 x 0.020 inch. One face is used for the thin-film components and active elements, with the edges utilized for the interconnection of submodules. Solder connection tabs are provided to facilitate the installation of diodes and transistors on the submodules. Submodules are provided for leads for connection to the flexible wiring board.

2.5 SUBMODULE LAYOUTS

The clock submodule layout is shown in Figures 3a and 3b. Component values are shown in Figure 2.

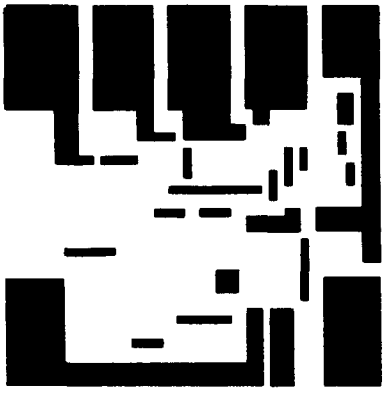

Figure 3a. Clock Solder Tabs and Conductor Pattern

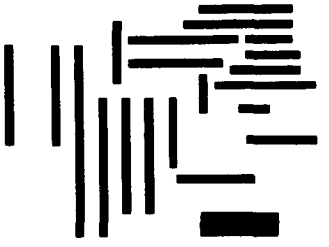

Figure 3b. Clock Resistor Pattern

Figure 3. Pattern for the Conductor and Tin Oxide Resistors Used in Making a Clock Substrate

The bistable submodule layout is shown in Figures 4a, 4b, 4c, and 4d. Component values are shown in Figure 2. The capacitor electrodes were placed on one section of the substrate to aid producibility.

The resistor pattern is obtained by photo-etching. Tantalum substrate electrodes are evaporated through a metallic mask. The chrome-gold for conductor and solder tabs is also evaporated through a metallic mask.

Electrolytic anodization is utilized to prepare a dielectric for the capacitors. Counter-electrodes of chrome-gold are evaporated through a metallic mask.

The capacitor submodule is fabricated by using an evaporated and anodized tantalum substrate electrode. Chrome-gold films are evaporated to provide conductors, solder tabs, and a counterelectrode.

2.6 TEST PROCEDURES

Several in-process tests are made. The resistance films are checked for the desired value of ohms per square. Visual and resistance tests are made after etching of the resistor pattern. Continuity, leakage, and visual tests are made after the chrome-gold film evaporations. The capacitor submodule is checked for leakage, capacitance, and loss factor.

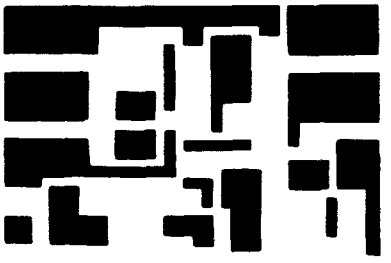

Figure 4a. Bistable Solder Tabs and Conductor Pattern

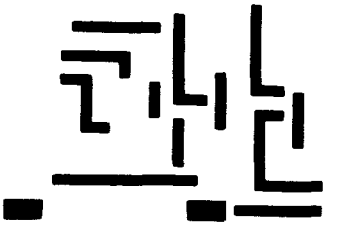

Figure 4b. Bistable Resistor Pattern

Figure 4c. Bistable Capacitor Tantalum Electrode Pattern *

Figure 4d. Bistable Capacitor Counter Electrode Pattern *

* The scale used for Figures 4c and 4d is one-half that used for Figures 4a and 4b.

Figure 4. Conductor, Resistor and Capacitor Pattern Used In Making a Bistable Substrate

Measurements are made of each passive component on the submodule and each diode and transistor is checked prior to assembly on the submodule. Each submodule is tested by itself before a complete set is assembled to form a staircase generator. Measurements such as square-wave input amplitude range permissable, square-wave amplitude output, saturation voltage at the collectors of bistable and clamp transistors and rise times were measured on each bistable submodule.

The following set of test specifications were set up to insure that each individual bistable submodule was satisfactory.

Measurement	Test Limits
1. At Trigger output (Supply voltage at 6)	
(a) Vces	0.1 v
(b) Vc	1.0 ± 5 %
(c) Tr	6 μ sec (max)
2. At Clamp output (with Clamp Diode open and Supply voltage at 6)	
(a) Vces	0.1 v
(b) Vo	5.6 ± 5 %
(c) Tr	20 μ sec (max)
At Clamp output (with Clamp Diode closed using test zener)	
Vo	2.4 ± 0.07
3. With nominal trigger of 1.0 v peak, device will remain operating as the supply voltage is varied from 4.8 to 7.2 v (6.0 ± 20 %).	
4. With nominal supply voltage of 6.0 v, device shall remain operating as the trigger voltage is varied from 0.75 to 1.25 v peak.	

After assembly into a complete module, a set of data was taken to evaluate the over-all performance of the staircase generator. Data is taken at nominal supply voltage and at the extremes of the supply voltage. Table 1 shows the actual readings taken from the three delivered modules.

The terminal arrangement on the flexible board extending out of the cans is as follows (left to right):

1. Output from bistable No. 6 (labeled spare)
2. Spare
3. Clock output
4. Zener voltage output

5. + 6 volt supply
6. Output (stairstep voltage)
7. Common (ground)
8. Spare

The first delivered module (serial No. 1) is marked with a blue dot; the next two are identified by serial numbers 3 and 4.

TABLE 1. MEASUREMENTS MADE ON THE THREE DELIVERED MODULES

Quantity	Module No. 1			Module No. 3			Module No. 4		
Supply voltage (volts)	4.8	6.0	7.2	4.8	6.0	7.2	4.8	6.0	7.2
Total Current Drain (ma)		7.0			6.2			7.1	
*Staircase Total Output Voltage (millivolts)	84	88	92	85	88	92	83	86	88
*Clock Output Voltage (volts P - P)	0.75	0.95	1.15	1.18	1.5	1.8	1.17	1.48	1.79
*Clock frequency (cps)		91			28.3			45.7	
*Bistable No. 6 Output (volts P - P)	0.97	1.0	1.02	0.95	1.0	1.1	0.98	1.0	1.02

*Indicates measurement with a Tektronix Scope to an estimated accuracy of ±10 per cent. D-C readings are to an accuracy of ± 5 per cent.

SECTION 3

3. PACKAGING, INTERCONNECTIONS, AND THERMAL DESIGN

To provide the desired accessibility and flexibility, the module is fabricated using a flexible printed wiring board folded 180 degrees over a center silastic core. Nine submodules are attached to the outside surface of the board, and seven conventional electrical components are attached to the underside at one end of the board. The opposite end of the board is cut away to allow access to the conventional components from both sides after the flexible board is folded. Figure 5 shows the layout of the flexible printed wiring board supporting and interconnecting the submodules, and Figure 6 is an assembly sketch of the complete module. Input and output connections are provided on a tab extension of the printed wiring board.

3.1 SUBMODULE ASSEMBLY

The assembly of active elements on a substrate is accomplished in a two-step process. First, fine wires are soldered to all points that must be connected to either diodes or transistors. Next, heavier wires are soldered to all points requiring external connection. The surface of the substrate is then covered with a 10-to15-mil thick layer of encapsulant. This layer is allowed to cure. The diodes and transistors are then soldered to the proper wires and a second layer of encapsulant is applied to protect the active elements and the wiring.

The submodules of units one and three were encapsulated with a silicone varnish whereas the submodules of unit 4 (except for the clock) were encapsulated in an epoxy resin.

3.2 MODULE ASSEMBLY

The set of submodules is fastened to the flexible printed circuit board with a silastic adhesive and the external leads are soldered to the proper points on the printed circuit pattern. The adhesive can be stripped from the board so that entire submodules can be replaced if necessary.

The complete circuit board assembly is then encapsulated in its shell of silicone rubber within the outside metal case. Figure 7 shows the disassembled module consisting of metal cover, base plate with silicone rubber, silicone rubber shroud and printed circuit board assembly. The process used permits disassembly into the pieces shown without damage to any of the encapsulation. When assembled in its metal case, the unit is very well protected from shock and vibration.

Figure 8 is a view of the front of the flexible wiring board assembly. Reading clockwise from the upper left, the arrangement of this assembly is as follows:

1. Commercial components (precision resistors and zener diode)
2. Bistable No. 6
3. Clock capacitor
4. Bistable No. 3

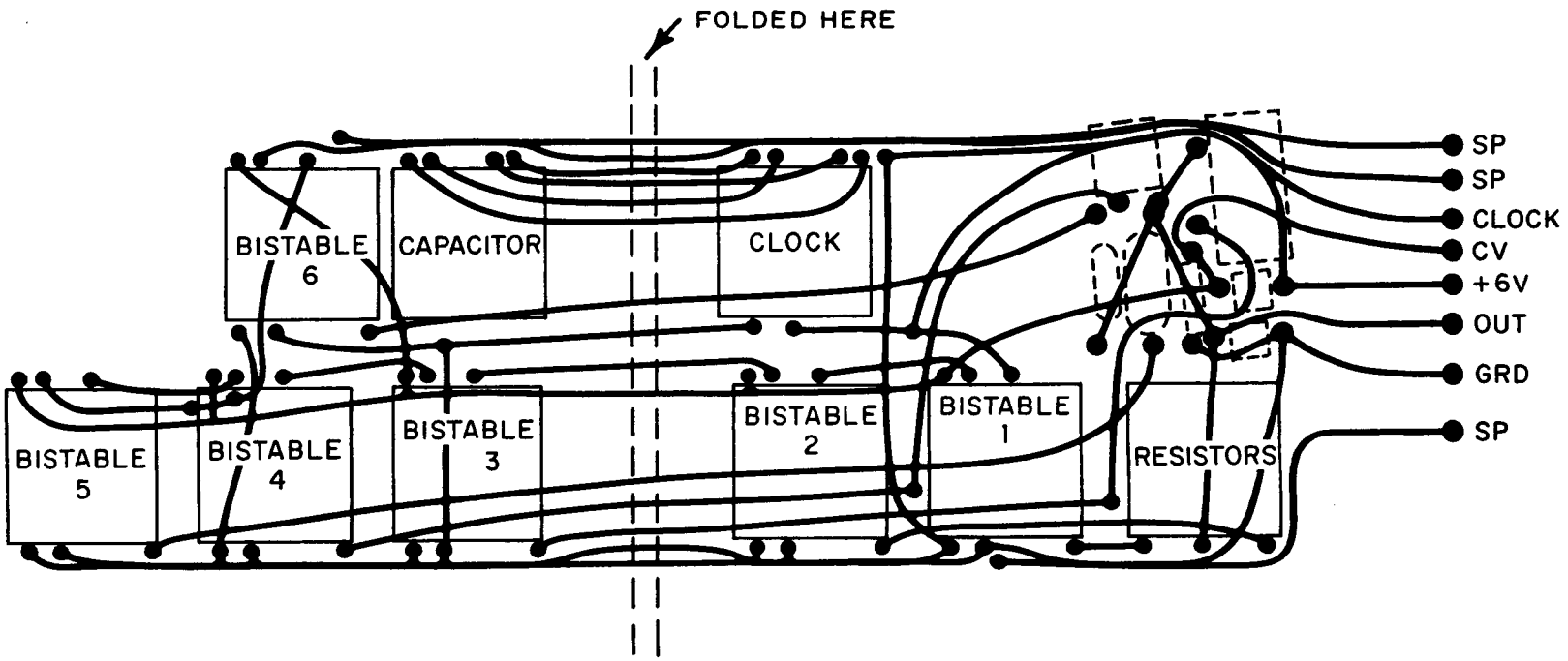

Figure 5. Layout of a Flexible Printed Wiring Board

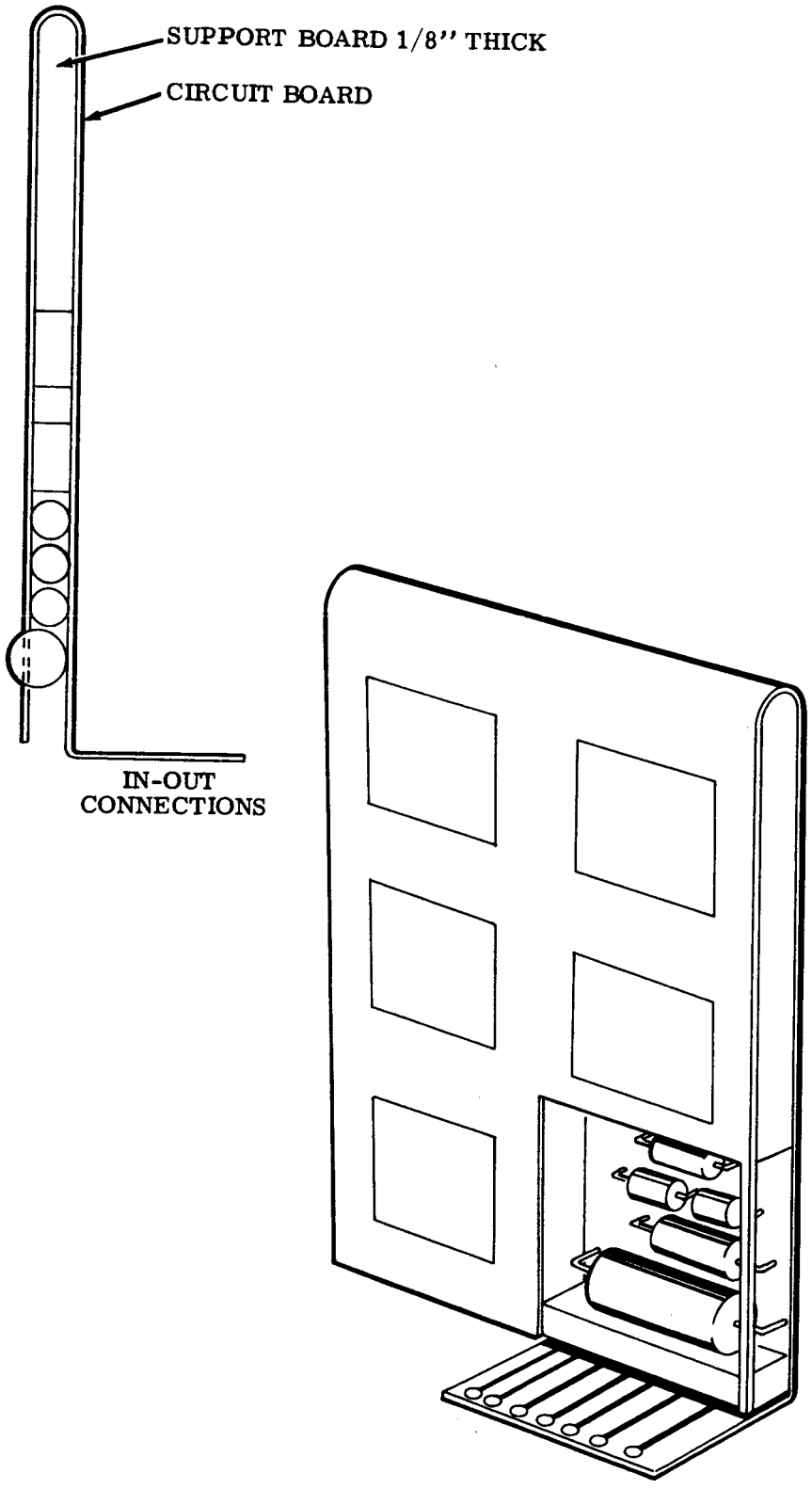

Figure 6. Sketch Showing the Use of Flexible, Printed Circuit Board

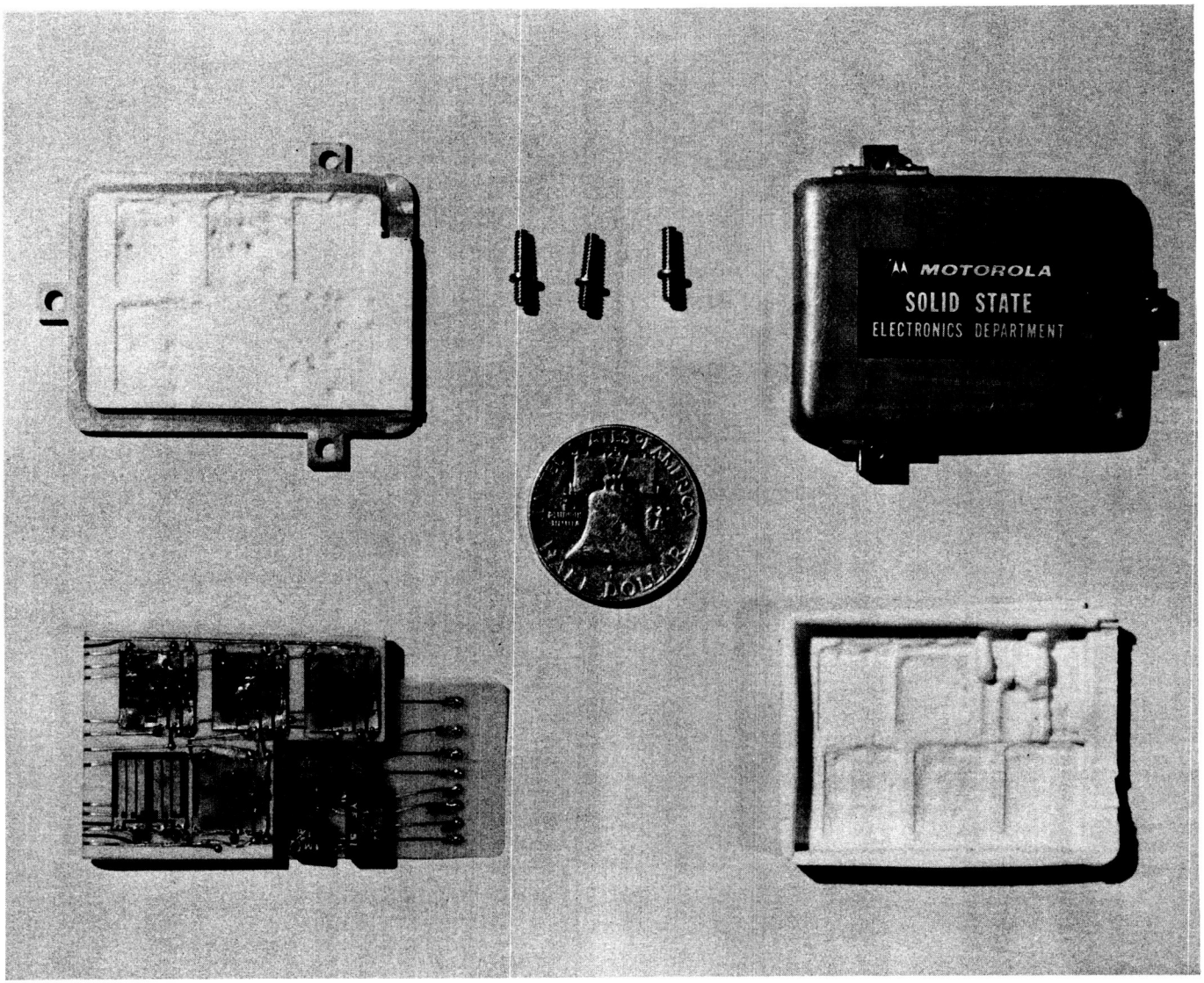

Figure 7. Disassembled Voltage Staircase Generator

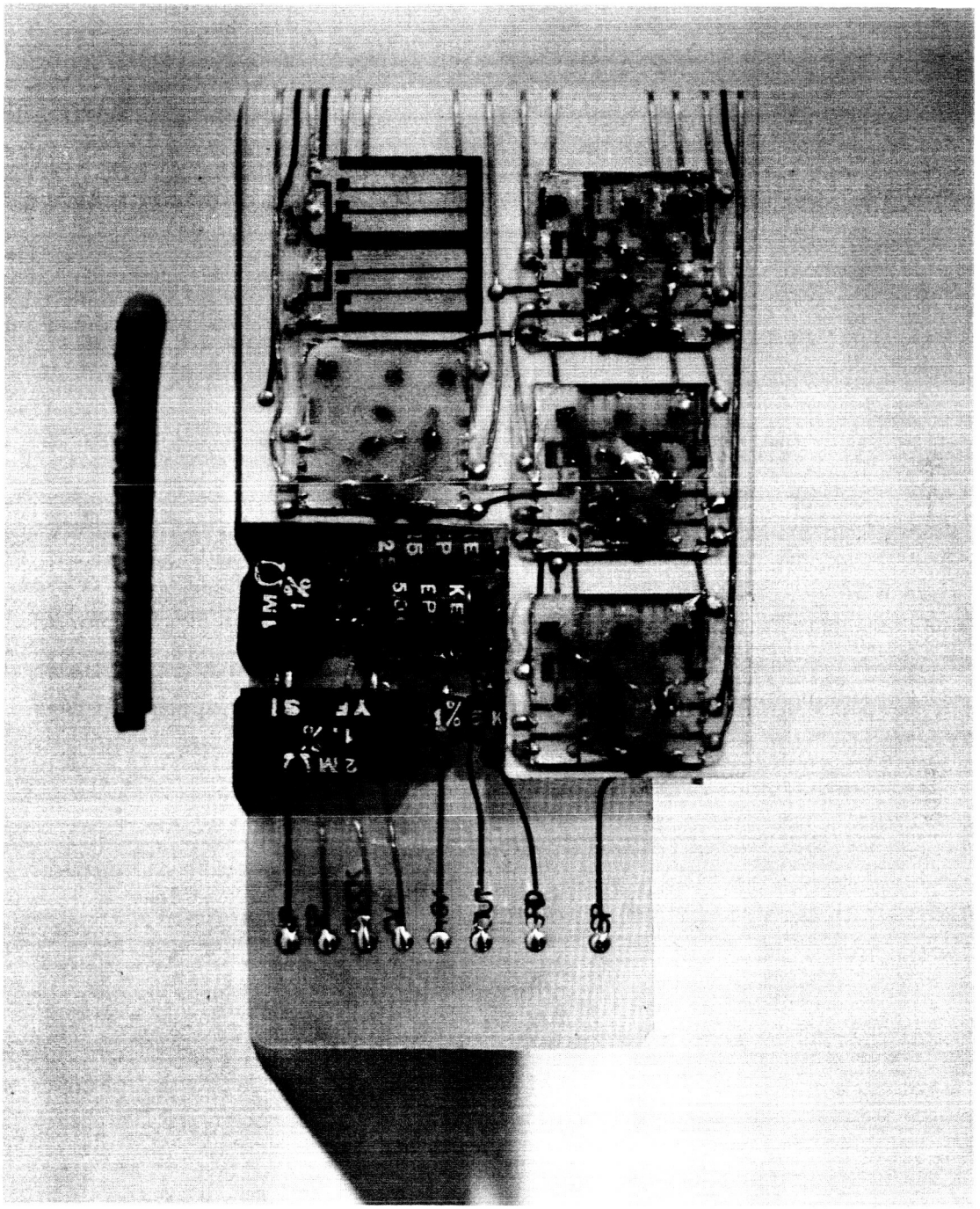

Figure 8. Front View of Flexible Wiring Board Assembly

5. Bistable No. 4

6. Bistable No. 5

Figure 9 is a view of the rear of the flexible wiring board assembly. Reading clockwise from the upper left, the arrangement of this assembly is as follows:

1. Clock submodule

2. Unused space

3. 8-and 4-megohm resistors

4. Bistable No. 1

5. Bistable No. 2

3.3 THERMAL CONSIDERATIONS

Temperature rises within this package will be moderate because of the low power dissipation of the circuit. At a supply voltage of 6 volts and a current drain of 7.1 milliamperes, the total dissipation is 42.6 milliwatts. With this amount of dissipation, it is estimated that the surface of the module will rise by somewhat less than 3 degrees C above the ambient temperature.

The transistors in the circuit are all being operated at very low dissipation levels. It is estimated that the power dissipated per transistor is about 0.02 milliwatts. This will vary considerably with the saturation voltage and the base-to-emitter voltage. With this level of power dissipation, the temperature rise of the junction should be less than 1.5 degrees C above the temperature of the surrounding encapsulation.

Therefore it appears that the transistor junctions will only be 4 or 5 degrees C above the ambient temperature.

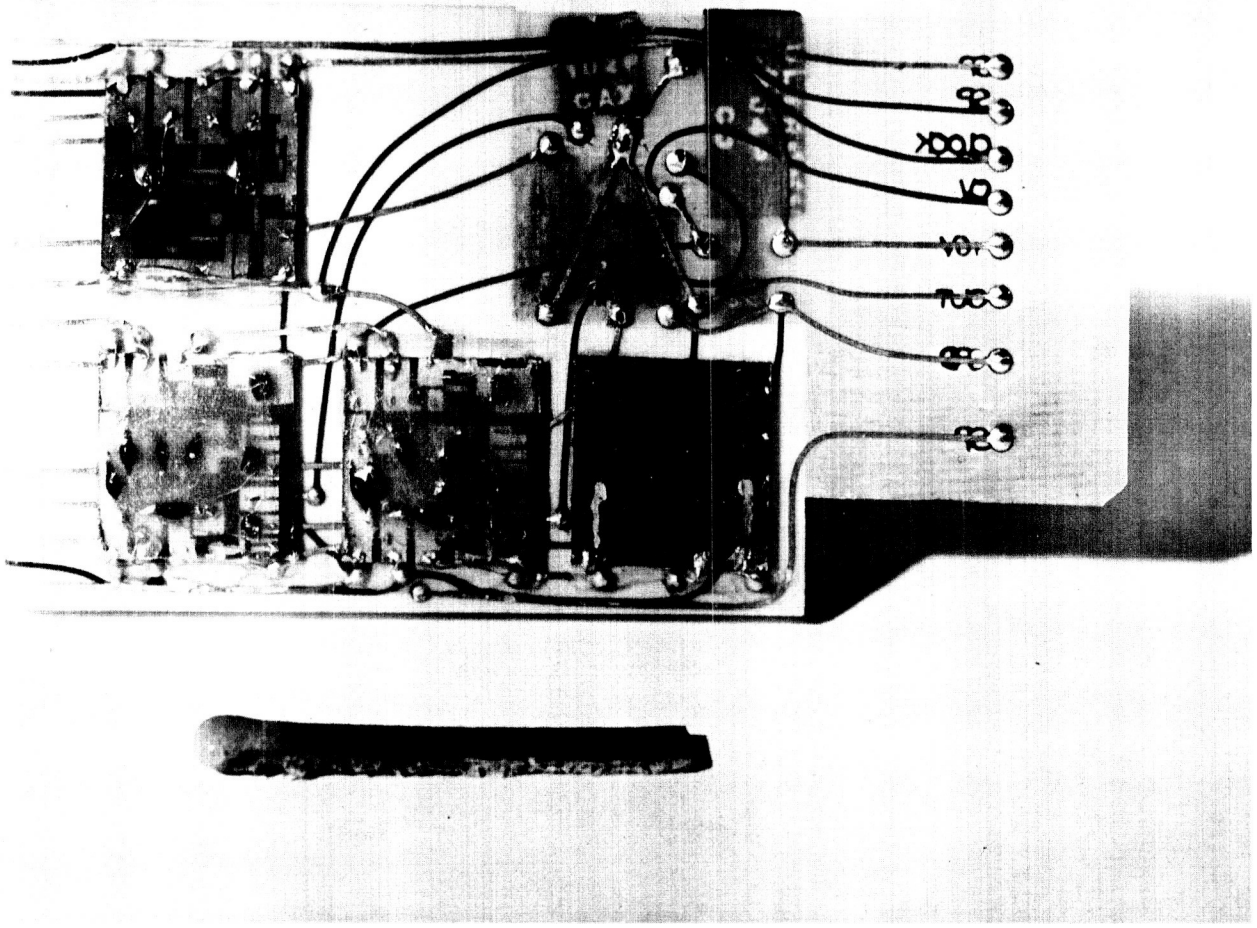

Figure 9. Rear View of Flexible Wiring Board Assembly

SECTION 4

4. PROBLEM AREAS

Several problems arose during the process of fabricating the three staircase generators. These problems can be divided into two classes: (1) problems that were solved in the process of building the three modules, and (2) problems that were uncovered but not solved.

4.1 PROBLEMS THAT WERE SOLVED DURING FABRICATION

The bistable circuit, as originally planned and laid out, used silicon dioxide capacitors. Difficulties were encountered in fabricating these capacitors and it was necessary to replace the silicon dioxide capacitors with tantalum capacitors. This change made it necessary to revise the circuit layout; the old layout was modified as little as possible and the new layout was not optimized from the standpoint of wiring ease.

At one point in the manufacturing process, the yield of tantalum capacitors became very poor. This trouble was finally traced to organic contaminants in the vacuum chamber used to deposit tantalum.

Early in the fabrication phase, the tin oxide resistors being used tended to show poor aging characteristics. To overcome this problem, the resistor process was altered to provide tin oxide resistors with antimony doping. This change gave thicker films for the same ohms-per-square value of resistance. The antimony-doped films have better aging characteristics and negative temperature coefficients.

A problem arose from the tendency for parts and wires to move within the encapsulant. Poor reliability resulted because of inadequate protection of the wiring on top of the thin-film circuit. This problem was solved by changing the encapsulant from a silicone varnish to an epoxy resin. This epoxy resin (used only on Serial No. 4) will stand a temperature of 125 C. If repairs are necessary, the resin can be removed with a soldering iron at 200 C; at this temperature the resin crumbles and can be readily removed from small areas with the tip of the iron.

4.2 PROBLEMS THAT WERE NOT SOLVED WITH THE FIRST THREE UNITS

4.2.1 High Temperature Operation

Tests indicate that this circuit operates marginally above an ambient temperature of 55 to 60 C. This apparently is due to the design of the circuit rather than the use of thin-film construction. A brief investigation reveals that the output voltage of the bistable decreases with temperature. This occurs because both the base-to-emitter voltage and the forward drop across the coupling diode decrease with increasing temperature. At about 60 C, the bistable output voltage has fallen to 0.75 volts, which produces marginal triggering of the next stage.

4.2.2 Circuit Layout

As mentioned in Paragraph 4.1, the layout went through at least one major change during the fabrication process. The resulting circuit layout was not optimized with respect to

transistor and diode placement. Because of wiring difficulties, the circuit reliability is decreased. In addition, circuit crowding could be helped by using much smaller diodes.

4.2.3 Tolerance Problems and Over-all Accuracy

A detailed study should be made to determine the over-all accuracy to be expected as a function of component tolerances and temperature. It appears very difficult to hold tolerances as tight as 5 per cent on each individual voltage step since these steps are affected by both transistor saturation voltage and diode conductance. The detailed analysis would indicate what tolerances could be held with practicable limits on saturation voltage and diode conductance.

4.2.4 The Packaging Problem

The present packaging method is a compromise between volumetric efficiency and accessibility. Additional work on the packaging problem could very probably reduce the size considerably and still retain accessibility.

4.2.5 Reliability

It is evident from the many changes that occurred during the fabrication of the first three units, and from the problems that had to be solved during this process, that these units should not be used to form an opinion of thin-film circuit reliability. To obtain a true picture of reliability, a large number of units must be fabricated under identical and closely controlled conditions. In addition, evaluation of the thin-film processes are continually resulting in improvements in reliability. For instance, since the delivery of Serial No. 4, it has been possible to increase the life of the tantalum capacitors at elevated temperature by several times. This improvement should be made prior to a reliability evaluation.

SECTION 5

5. CONCLUSIONS

Thin-film integrated circuit techniques developed at Motorola have been applied to the construction of a staircase voltage generator circuit. This application demonstrates the feasibility of this type of construction and indicates the degree of miniaturization possible with these techniques. The objectives as outlined in Paragraph 1.1 have been achieved except for a meaningful demonstration of reliability. Also, the feasibility of a packaging technique that protects the thin-film circuit and provides the possibility of repair has been shown.